

Soft Error Hardening for Asynchronous Circuits

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Abstract

As the devices are scaling down, the combinational logic will become susceptible to soft errors. The conventional soft error tolerant methods for soft errors on combinational logic do not provide enough high soft error tolerant capability with reasonably small performance penalty. This paper investigates the feasibility of designing quasi-delay insensitive (QDI) asynchronous circuits for high soft error tolerance. We analyze the behavior of Null Convention Logic circuits in the presence of particle strikes, and propose a novel technique to improve the robustness of threshold gates, which are basic components in NCL, against particle strikes by using Schmitt trigger circuit and resizing the feedback transistor. Experimental results show that the proposed threshold gates do not generate soft errors under the strike of a particle within a normal energy range if a proper transistor size is applied. The penalties, such as delay and power consumption, are also presented.

1. Introduction

When a high-energy particle, such as alpha or neutron, hits the silicon substrate of a CMOS chip, it can generate electron-hole pairs and form a short-duration current that can change the output of a gate [1]. A soft error occurs when this corrupt output is captured by a memory cell, register, latch, or flip-flop. The soft error is also often referred to as a single event upset (SEU).

While error correcting codes are successfully used, as a system solution, to protect memories against particle strikes, no such quick fix exists yet for combinational logic. In recent years, with the continuous scaling down of Very Large Scale Integrated (VLSI) circuits, attention on soft error has shifted from memories to combinational logic circuits [2] [3]. P. Shivakumar [2] predicted that the soft error rate (SER) per chip of logic circuits would increase by nine orders of magnitude from 1992 to 2011 due to technology scaling, and, at that point, would be comparable to the SER per chip of unprotected memory elements.

While most of researchers investigate the soft error issues in traditional synchronous circuits, little attention has been paid to asynchronous circuits. At first glance, asynchronous circuits seem more vulnerable to radiation-induced soft errors than traditional synchronous circuits because any signal transition is treated as an event in asynchronous circuits. In fact, quasi delay insensitive (QDI) asynchronous circuits have a strong potential for soft error tolerance. The combination of handshaking protocol and dual-rail encoding in QDI circuits provides the circuits with a potential capability to detect and correct the soft errors. Besides single event upsets, particle strikes may cause other malfunctions on a chip: charges induced by particle strikes may slowly accumulate in the substrate of a chip. Those long-term dose effects usually cause parameter shifts, in particular threshold voltages, which affect the timing of the system. QDI circuits are very robust to timing variation.

Monnet et.al proposed a metric, *sensitive time*, to evaluate the sensitivity of asynchronous circuits to transient faults [4]. Jang et.al proposed several SEU-tolerant QDI

circuit designs which cause the circuits to become three times larger and twice slower [5]. Peng et.al developed an efficient concurrent failure detection method for pipelined asynchronous circuits so that the asynchronous circuits halt in the presence of failure by single stuck-at faults or single event upsets [6].

Null Convention Logic (NCL) is a new design paradigm for QDI circuits [7]. Kuang et.al improved the soft error tolerance by modifying the NCL pipeline architecture to stop some soft error propagating [8]. This paper will present a technique to suppress the soft error generation at circuit-level. The proposed technique employs Schmitt trigger to achieve sufficient amount of soft error suppression with very small area, power and delay overhead.

The rest of this paper is organized as follows: Section 2 presents the background related to NCL and particle strike. Section 3 describes the behavior of NCL circuits in the presence of particle strike. Section 4 explains our proposed designs, and the experiment results are given in Section 5. Section 6 concludes the paper.

2. Background

2.1 Null Convention Logic

In this paper, QDI circuits are implemented using a class of threshold gates with hysteresis, proposed by K. M. Fant [7]. This implementation style is called Null Convention Logic (NCL). Fig. 1 shows the NCL pipeline architecture. The circuit consists of m -of- n threshold gates with hysteresis (TH mn), where n is the number of inputs and m is a threshold. An m -of- n threshold gate with hysteresis will set its output high when any m inputs have gone high and it will set its output low when all its inputs are low. For instance, the schematic of TH23 is shown in Fig. 2. A general method of designing any TH mn gate can be found in [9].

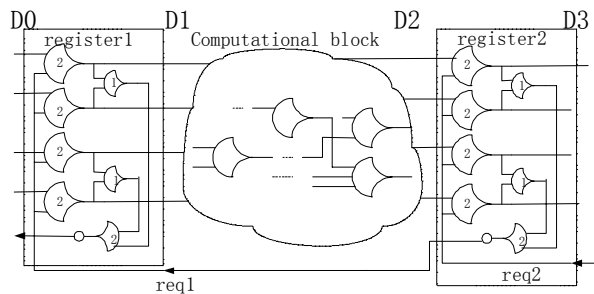


Fig. 1 NCL pipeline architecture

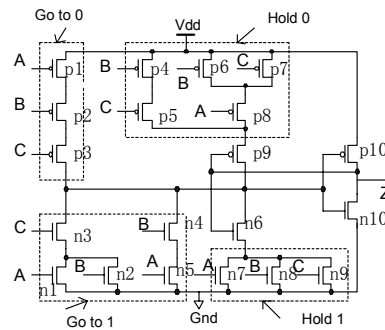


Fig. 2 Schematic of TH23 gate

NCL circuits use two completeness criteria to achieve its quasi delay-insensitive behavior. These two criteria are symbolic completeness of expression, and completeness of input. A symbolically complete expression is defined as an expression that only depends on relationships of the symbols presented in the expression. Specifically, the dual-rail encoding is a symbolically complete expression, as shown in Table 1, where each logic bit is represented by two wires.

The second criterion, completeness of input, imposes two behavior constraints on computational blocks: 1) the outputs may not transition from all NULL to a complete set of DATA until the input values are completely DATA; and 2) the outputs may not transition from a complete set of DATA to all NULL values until the input values are completely NULL. By observing these two criteria, dual-rail AND, OR and full adder can be designed as shown in Fig.3. Any complex computational block can be built using these basic dual-rail gates. Due to the hysteresis of threshold gates, in a computational block, the

number of gate output nodes with high voltage monotonically increases during the computation, i.e. transition from NULL to complete DATA.

Table 1 Dual-rail encoding

Dual-rail encoding (D ¹ , D ⁰)	Information (DATA level)
(0, 0)	NULL
(0, 1)	Logic "0"
(1, 0)	Logic "1"
(1, 1)	invalid

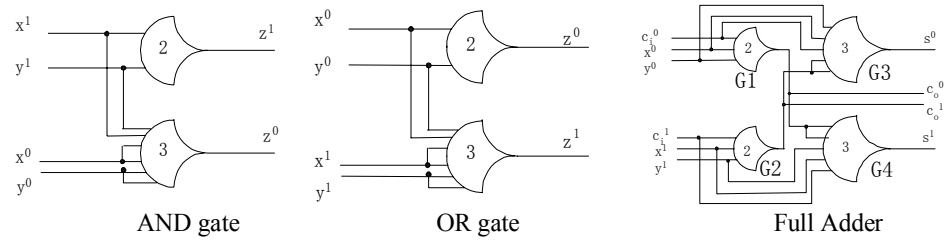


Fig. 3 Dual-rail AND, OR and full adder.

The registers between computational blocks are used to coordinate the four-phase protocol communications. First, a register detects the completeness of delivered data and inform the preceding register of the completeness. Secondly, the registers function as switches controlling the DATA and NULL flow. Specifically shown in Fig.1, if the request signal *req2* from the following stage is high to request Data, then Data are allowed to pass through register 2, and after a complete set of Data pass through register 2, the request signal *req1* will become low to request Null from the preceding stage, which means the computation in the current stage is finished and the circuit needs to be reset. A similar operating mode exists when the request signal *req2* from the following stage is low to request Null.

2.2 Particle Strike Modeling

Fig.4 shows the mechanism of soft errors in semiconductor circuits. Electron hole pairs with a very high carrier concentration are generated as particles lose energy in silicon, and the resulting charges can be rapidly collected by the electric field, creating a large current transient at that node. An SEU occurs when enough charge is collected in such a short time to reverse or flip the data of a gate output, memory cell, register, latch, or flip-flop. The transient current due to a particle strike can be modeled as [10]

$$I(t) = \frac{2Q}{T\sqrt{\pi}} \sqrt{\frac{t}{T}} \cdot \exp\left(-\frac{t}{T}\right) \tag{1}$$

where Q is the amount of collected charge, and T is a process technology-dependent time constant. A transient current is plotted in Fig.4 for Q=60fC and T=20ps.

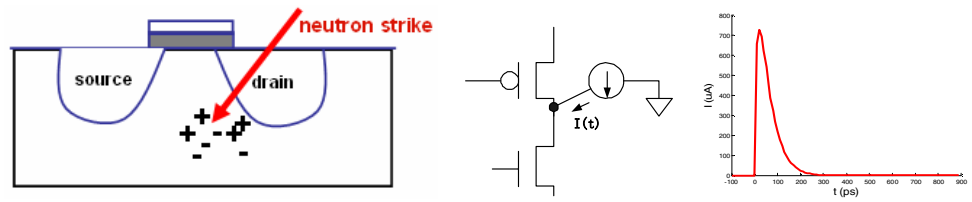


Fig. 4 Mechanism of soft errors in semiconductor circuits

Whether the current is injected into or removed from the node depends on the type of victim drain. For example, a current is injected into the node if a particle hit occurs at a p-type drain, therefore momentarily increasing the node voltage. If the logic value of the node is 0 and the current is injected to the node, a 0-1-0 glitch may occur. Similarly, a 1-0-1 glitch may be generated if an n-type drain is hit.

3. Soft Error in Null Convention Logic

3.1. Soft Error in NCL computational blocks

The mechanism shown in Fig.4 can be applied to NCL circuits hit by particles. However, due to the hysteresis of threshold gates and dual-rail encoding, NCL circuits have very different behavior than traditional synchronous circuits in the presence of particle strikes.

First, we consider the soft error generation at the output of an individual threshold gate. Theoretically, there are four types of soft errors that may be generated at the gate output when a particle hit different transistors inside the threshold gate. These four types are: positive glitch (0-1-0), negative glitch (1-0-1), positive fault transition (0-1), and negative fault transition (1-0). The specific type of soft error depends on the input pattern, present output, and the location of the particle strike. For example, when the input pattern of a TH23 gate is ABC=000 and the drain of NMOS transistor n6 (or n3 or n4) is hit (shown in Fig. 2), a positive glitch (Fig. 5(a)) may be generated at the output. If ABC=001 and output is 0, the same strike may result in a positive fault transition (Fig. 5(c)). Fig. 5 lists possible soft errors generated at TH23 output if a particle hit a proper transistor.

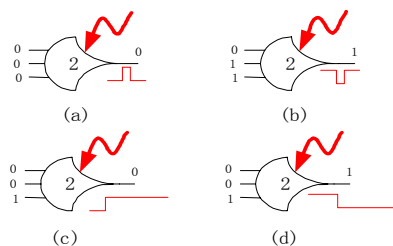


Fig. 5 Soft error generation in TH23 gate.

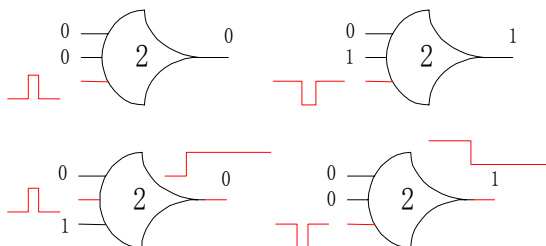


Fig. 6 Glitch soft error propagation

Then, we investigate the soft error propagation in a network of threshold gates – a computational block. Due to the hysteresis, a generated glitch (0-1-0 or 1-0-1) will be either filtered or transformed into a fault transition (0-1 or 1-0) immediately by the following gate, as shown in Fig. 6. And then the resulting fault transition (0-1 or 1-0) conditionally propagates through the next gates. Therefore only **static** fault transitions (0-1 or 1-0) may arrive at the output of computational block.

3.2. Soft Error in NCL Pipelines

Unlike traditional synchronous circuits, there is no global clock in NCL circuits. The delivery of the computation results from one stage to the next stage is implemented by the handshaking scheme. Let us focus on register 2 in Fig. 1. The timing diagram of register 2 is shown in Fig. 7. “NULL” in Fig. 7 means that all dual-rail bits are Null, and “DATA” means that all dual-rail bits are valid logic values (logic “0” or logic “1”). T1 denotes the duration of “DATA” with high req2, and T2 is the duration of “DATA” with low req2. Based on the timing diagram, the following scenarios can be obtained.

Scenario 1: During the “NULL” period of D2, no soft error appears at D2. In this case, the only possible soft error is a glitch (0-1-0), and this soft error can not propagate because the inputs of all gates are completely zero.

Scenario 2: During the “DATA” period of D2, only soft errors within time slot T1 will propagate to the next stage. This implies that soft errors at D2 during T2 will be blocked, and therefore can be ignored.

Scenario 3: A 1-0 fault transition at D2 occurs only when the computational block is transitioning from “DATA” to “NULL”. A 1-0 fault transition may only lead to premature firing, and therefore will not affect the circuit logic function.

In summary, a particle strike on NCL computational block may generate one of four types of soft errors at the victim gate output, but only fault transitions (0-1 or 1-0) may appear at the output of computational block. Only positive fault transitions (0-1) during T1 at the output of computational block may lead the circuit to fail.

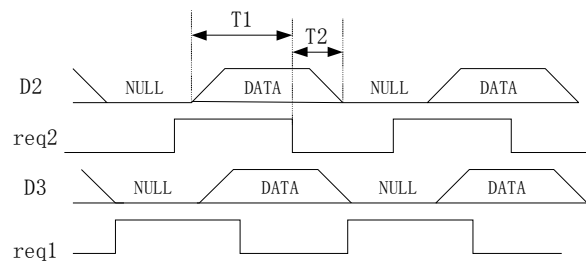


Fig. 7 Timing diagram for NCL pipeline

4. Soft Error Hardening Technique

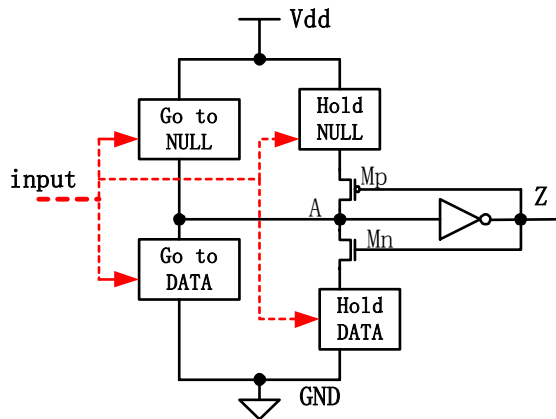


Fig. 8 Threshold gate by Sobelman[9]

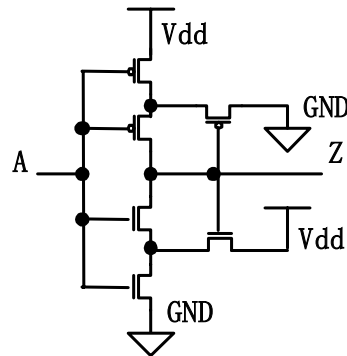


Fig. 9 Schmitt trigger

Based on the analysis in Section 3, only positive glitch (0-1-0) and positive fault transition (0-1) may eventually affect the logic function of the NCL circuits. The general structure of a static m -of- n threshold gate with hysteresis was proposed by G. Sobelman [9], shown in Fig. 8. These two soft errors are induced by particle strikes either on the drain of any NMOS transistor connected to node A or on the drain of the PMOS in the inverter. Simulation shows that the drain of the PMOS in the inverter is much less sensitive to particle strike than the drain of NMOS connected to node A. Therefore, a negative transient pulse at node A is the major reason for the soft error at output Z.

In our approach, a Schmitt trigger is used to replace the inverter in Fig. 8 to block the negative transient pulse at node A due to particle strike. A typical Schmitt trigger is double-side, shown in Fig. 9. Fig. 10 shows the threshold gate with double-side Schmitt trigger. This Schmitt trigger can block both negative and positive transient pulse at its input. Because only negative transient pulse is required to be blocked, a single-side Schmitt trigger, instead of a double-side Schmitt trigger, can be used to achieve the required transient pulse blocking purpose with lower delay and power overhead, as shown in Fig. 11.

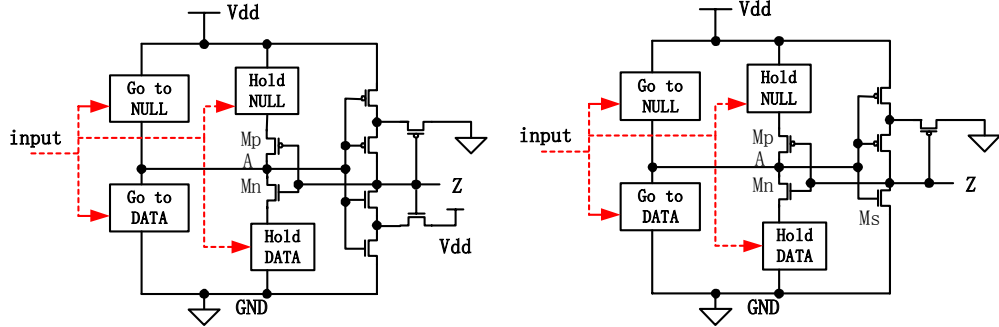


Fig. 10 Threshold gate with double-side Schmitt trigger Fig. 11 Threshold gate with single-side Schmitt trigger

5. Experimental Results

In order to evaluate the effectiveness of the proposed soft error hardening technique, we have performed the experiments on TH23 gate, and have compared the results of different implementations. In our experiment, every circuit is designed in a $0.25\mu\text{m}$ CMOS technology and simulated by Cadence SPECTRE with supply voltage 2.5V. All transistors (NMOS or PMOS) have a channel width of 450nm and a channel length of 300nm except stated otherwise. Fig. 12 shows a soft error occurrence model used in our threshold gate with single-side Schmitt trigger. The same model is applied to other implementations of threshold gate in our experiment. The load capacitor is set to 25 fF. A pulse current source I is connected to node A to mimic the effect of particle strike. When the output Z is low, a pulse current at A may result in a glitch (0-1-0) or a fault transition (0-1), as shown in Fig. 13. For TH23 gate, when ABC=000 and Z=0, the possible soft error is a glitch; when ABC=001 and Z=0, the possible soft error is a static soft error (0-1).

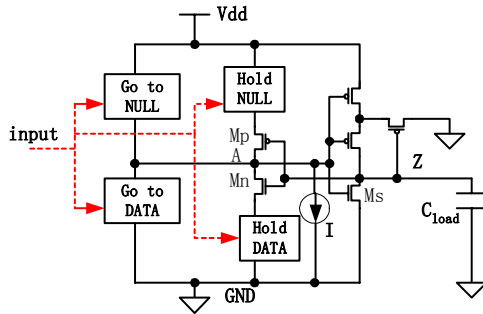


Fig. 12 Soft error model

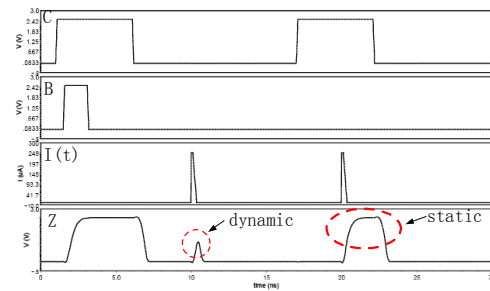


Fig. 13 Soft errors for TH23 with A=0

5.1 Transient Current Model

A transient current source can be used for soft error simulation, as shown in Fig.12. The current $I(t)$ is modeled by equation (1), where two parameters, T and Q are needed to determine current $I(t)$. T depends on semiconductor process, and Q is proportional to particle energy. The T for $0.25\mu\text{m}$ CMOS is assumed to be 80 ps, and the typical range of Q is from 20 fC to 120 fC. For simplicity, we use a trapezoid pulse current to approximate $I(t)$,

as shown in Fig.14. In our experiments, $t_r=20\text{ ps}$, $t_f=250\text{ ps}$, $p_w=100\text{ ps}$. I_{max} is linearly proportional to Q , modeled as $I_{max}=5Q\text{ uA}$. For example, $I_{max}=400\text{ uA}$ corresponds to $Q=80\text{ fC}$.

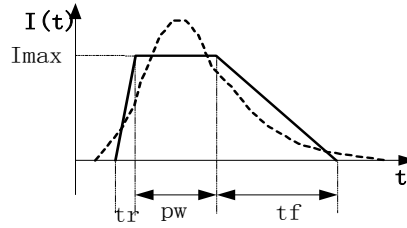


Fig. 14 Trapezoid approximation for pulse current

5.2 Simulation Results

To demonstrate the performance of the proposed technique, we simulated three different implementations of TH23 gate: basic (Fig.8), single Schmitt (Fig. 11) and double Schmitt (Fig. 10). For each of them, three different widths ($0.9\text{ }\mu\text{m}$, $1.8\text{ }\mu\text{m}$ and $3.6\text{ }\mu\text{m}$) for the **feedback PMOS transistor M_p** are used. Therefore, nine circuits are simulated and compared. To effectively compare the single Schmitt and the double Schmitt, we set the NMOS transistor M_s in single Schmitt (Fig. 11) as three times big ($1.35\text{ }\mu\text{m}$) as one NMOS (450 nm) in the double Schmitt so that they consume the same area. All other transistors have the same size ($W=450\text{ nm}$, $L=300\text{ nm}$).

A) Sensitivity to particle strike

To measure the sensitivity of each circuit to particle strike, two current pulses are generated to mimic particle strike: one at $ABC=000$, and another one at $ABC=001$ and $Z=0$. The former may create a dynamic glitch, and the later may lead to a static soft error, as shown in Fig.13.

Fig.15 plots the dynamic glitch magnitude as a function of Q (or I_{max}) for different circuits. For example, “*single1.8*” means the design with single-side Schmitt trigger and $1.8\text{ }\mu\text{m}$ wide feedback PMOS transistor. When Q is higher than 70 fC , the basic designs will generate big dynamic glitch that may eventually lead to a static soft error at the output of its succeeding gates. The dynamic glitches generated by the designs using Schmitt trigger are below 1 V even if Q is around 100 fC . Thus, the dynamic glitches in the proposed designs can be ignored.

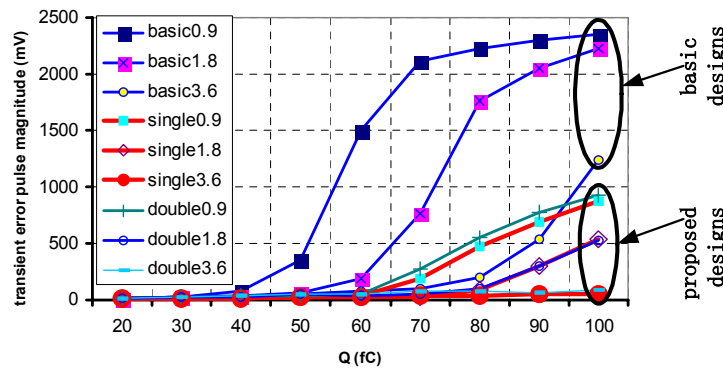


Fig. 15 Dynamic glitch magnitude

However, a static soft error will occur when Q is more than a threshold Q_{max} , even for the proposed designs. It is obvious that the bigger the Q_{max} , the more robust the circuit. To find Q_{max} , during simulation we increase I_{max} of the pulse current source until a static soft error occurs. The Q_{max} corresponds to the maximum I_{max} which does not cause a static soft

error. The Q_{max} is plotted in Fig.16 for nine circuits. From Fig.16, two conclusions can be drawn: 1) increasing the feedback PMOS transistor can improve the robustness to particle strike; 2) both single and double Schmitt triggers significantly increase the maximum allowed Q without static soft error; and 3) single and double Schmitt triggers have very close impacts on the robust improvement, compared to basic design. Since the probability of Q more than 100 fC is very small, the static soft error in the proposed designs with 3.6 μm feedback PMOS can also be ignored.

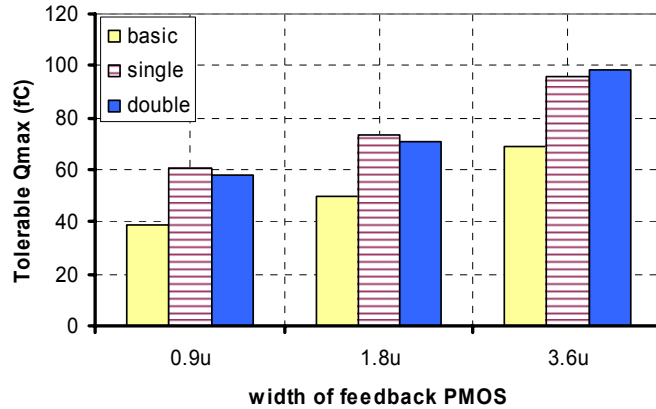


Fig. 16 Particle strike tolerance for different designs in terms of static soft error

B) Performance penalty

The proposed technique increases the insensitivity of threshold gate to particle strike. On the other hand, the penalties of the proposed technique include increased power consumption and increased delay. Fig. 17 shows the energy consumed by TH23 gate during a switch cycle. A switch cycle is defined as the time duration when the output of the gate transitions from 0 to 1, and back to 0. The circuits with single-side Schmitt trigger consume around 20% more energy than basic designs. The double-side Schmitt trigger doubles the energy consumption of the basic design.

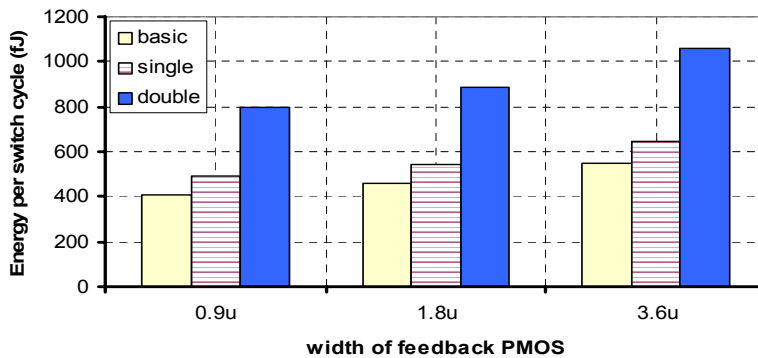


Fig.17 Power consumptions for different designs

Fig. 18 shows the rising, falling and average delays for each design. The rising and falling delays are measured by Cadence SPECTRE while the average delay is calculated by $(\text{rising delay} + \text{falling delay})/2$. The proposed technique imposes the average delay overhead. The double-side trigger increases the average delay by a larger amount than the single-side trigger. The single-side trigger increases the rising delay and decreases the falling delay, but the average delay is bigger than that of basic design. And also, for each specific design, increasing feedback PMOS transistor size will lead to an increased delay.

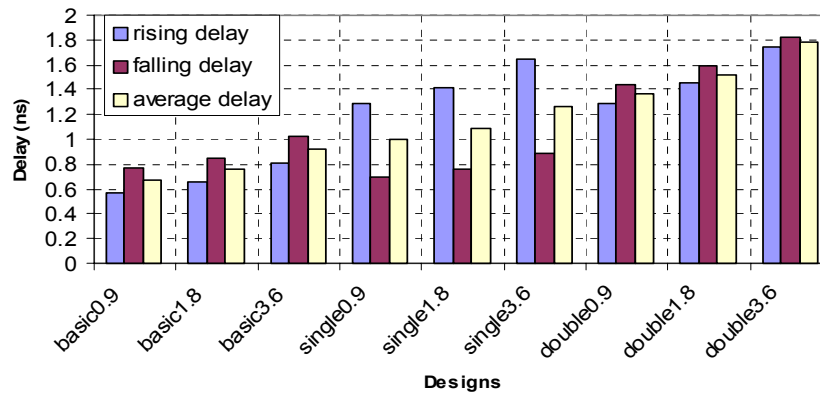


Fig. 18 Delays for different designs

C) Trade-off between soft error, power and delay

Based on the above simulations, the high tolerance of particle strike can be achieved by sacrificing the power and delay performance. To achieve the same particle strike tolerance, the single-side trigger designs sacrifice less than the double-side trigger designs do. For example, both *single3.6* and *double3.6* can suppress soft errors almost equally by 100%. The *double3.6* design increases power by 92.2% and average delay by 94.4% while the *single3.6* design increases power by 16.9% and average delay by 37.7%, compared to the *basic3.6* design. Therefore, designs with single-side Schmitt trigger are better than designs with double-side Schmitt trigger.

6. Conclusions

Radiation-induced soft errors threaten the reliability of digital systems as devices sizes are shrinking. In this paper, we have investigated the effect of soft errors in asynchronous circuits, and proposed a technique to suppress soft error generation at gate-level with small area, power and delay overhead. This technique employs single-side Schmitt trigger in threshold gates for Null Convention Logic, and achieves a sufficient amount of soft error suppression.

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