

Low Power Operation Using Self-Timed Circuits and Ultra-Low Supply Voltage

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ABSTRACT

In this paper, a self-timed architecture for low voltage low power design is proposed. Compared to synchronous circuits, self-timed circuits are more robust to ultra-low supply voltage. In many signal-noise-ratio (SNR)-required DSP applications, this robustness allows the circuit to operate with very low supply voltage, even if some data samples are missed due to this low voltage. These missed data are interpolated at the output. Simulation shows that a significant power saving can be achieved at an acceptable SNR loss in a case study—speech signal processing. This proposed low power method can be combined with many other low power schemes at various levels to achieve further power saving.

1. INTRODUCTION

Scaling of supply voltage leads to an aggressive power saving as well as an increased delay [1]. A lower bound of supply voltage $V_{critical}$ exists for the path delay corresponding to the throughput requirement. Erroneous operations probably happen when an ultra-low supply voltage (ULSV), a voltage less than $V_{critical}$, is applied. Fortunately, a moderate degradation due to the erroneous operations can be viewed as the introduction of noise, and thus is usually allowed in many DSP systems dealing with noise [2]. This fact leads to a tradeoff between the output signal-to-noise ratio (SNR) and power performance.

This tradeoff was implemented in synchronous DSP architectures in [3], referred to as soft digital signal processing. Consider the block diagram of a synchronous digital signal processing circuit shown in Fig.1, where the input/output registers are clocked at the sample period $T_s = 1/f_s$, where f_s is the sample rate. If the delay of a single full-adder is T_{FA} , then the critical path delay of the N-bit adder is given by $T_{critical} = N \cdot T_{FA}$. If $T_{critical}$ is increased beyond T_s due to the reduction of supply voltage for power saving, the outputs for some inputs are incorrect while the outputs for other inputs are still correct. The erroneous outputs will be detected and partially compensated for via DSP techniques. The reader is referred to [3] for detailed description and analysis of the erroneous operation due to ULSV in synchronous circuits. However, the application of this technique is limited by the following factors: 1) the applied circuit must have a characteristic of delay data-dependency; 2) the probability (frequency) of the erroneous outputs depends not only on the

supply-voltage but also on the distribution of inputs, and a high probability of the erroneous outputs may degrade the accuracy of the final outputs to an unacceptable degree even after compensation.

So far, no research on self-timed circuit under ULSV has been reported. In this paper, a self-timed architecture is proposed for low power design in DSP applications. The behavior of the architecture is investigated when an ULSV is applied. Simulation results show that significant energy saving can be achieved at the cost of less than -10 dB noise when the proposed architecture is used for speech signal processing.

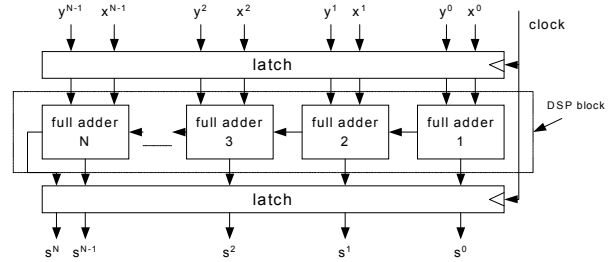


Fig.1 Block diagram of a synchronous DSP circuit

2. SELF-TIMED ARCHITECTURE

Before we focus on the analysis of the erroneous operation in self-timed circuit due to ULSV, a self-timed architecture is presented and the timing constraint for no error operation is discussed.

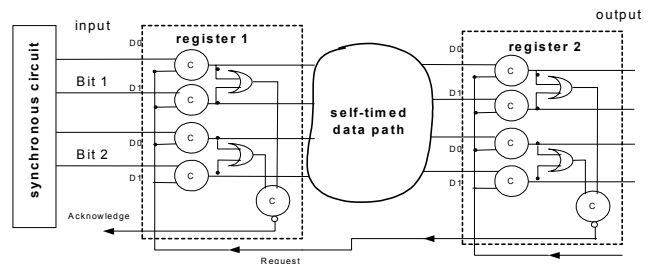


Fig. 2 A self-timed circuit receives data from a synchronous circuit (only two bits in data bus for simplicity)

The self-timed circuit to be addressed is speed independent, where each bit of the data is encoded by dual rails (D0, D1), shown in Fig. 2. Table 1 shows the dual-rail encoding scheme. The state DATA 0 (D0=1, D1=0) corresponds to a Boolean logic 0. The DATA 1 (D0=0, D1=1) corresponds to a Boolean logic 1. SPACER (D0=0, D1=0) corresponds to the empty set meaning that value of the bit is not yet available. The state (D0=1, D1=1) is forbidden.

Table 1 Dual-rail encoding scheme

Bit value	Rail logic value	
	D0	D1
DATA1	0	1
DATA0	1	0
SPACER	0	0
Invalid	1	1

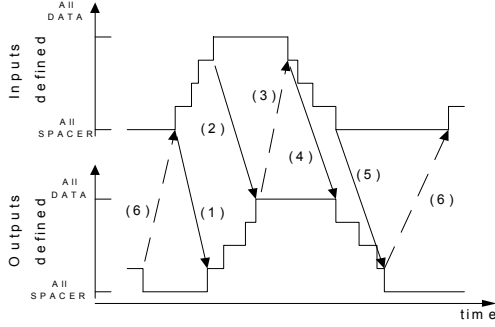


Fig.3 Seitz's weak condition

In order to achieve speed-independence, the data path must work under Seitz's weak condition [4], shown in Fig. 3. The orderings (1), (2), (4), (5) are guaranteed by the proper design of the data path while ordering (3) and (6) are realized by the register control.

Some techniques, such as differential cascode voltage switch logic (DCVSL) [5] and NULL convention logic (NCL) [6], can be exploited to design the dual-rail data path. Martin's delay-insensitive full adder [7] can also be used in the data path. Registers are dedicatedly designed for orderings (3) and (6) in Fig. 3. As shown in Fig.2, a register is composed of C-elements and OR gates. Considering register 1, if the request signal from register 2 is high to request DATA, then DATA is allowed to pass through register 1, and when each bit is DATA, the acknowledge signal will become low to request SPACER from the pre-stage, which means the computation is finished and the circuit needs to be reset. Similarly, if the request signal from register 2 is low to request SPACER, then SPACER is allowed to pass through register 1, and when all of bits are SPACERs, the acknowledge signal will become high to request another DATA from the pre-stage, which means the reset is finished and the circuit can start another computation.

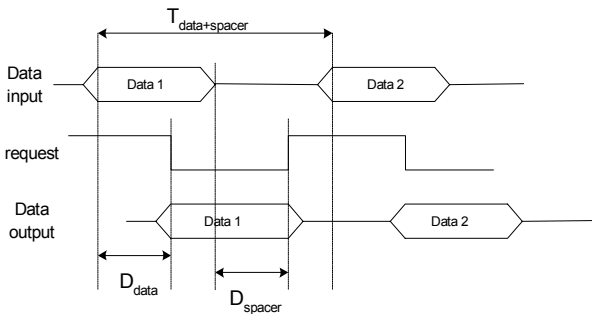


Fig.4 Timing constraint of self-timed circuit

In many applications, the input data of the self-timed come from a synchronous system, such as an A/D converter, and the data rate is constant and independent of the delay of the self-timed circuit. However, the allowed maximum input data rate is limited by the speed of the self-timed circuit. The timing constraint is illustrated in Fig. 4, where $T_{data+spacer}$ is the input

DATA-SPACER cycle, D_{data} is the propagation delay of data from register 1 to register 2, which includes the delays of two registers and the data path, similarly D_{spacer} is the propagation delay of spacer from register 1 to register 2. The sum of D_{data} and D_{spacer} must be less than or equal to $T_{data+spacer}$, i.e.,

$$T_{data+spacer} \geq D_{data} + D_{spacer} \quad (1)$$

Otherwise, the self-timed circuit will miss some input data (see Section III). Usually a speed margin is needed to guarantee that the self-timed circuit works correctly.

3. MISS RATE IN SELF-TIMED CIRCUITS

The effect of ULSV on self-timed circuit is totally different from that on synchronous circuit described in [3]. When an ULSV is applied to a self-timed circuit, inequality (1) is violated. The following analysis shows that under the condition of ULSV the self-timed circuit would miss some input samples (DATA or SPACER), and the outputs corresponding to the inputs not missed are always correct. In other words, an output is either lost or delivered correctly.

For the sake of simplicity, we make the following assumptions:

- 1) The data rate of input is fixed, and the duration of DATA is equal to that of SPACER, i.e., $T_{data} = T_{spacer} = 0.5T_{data+spacer}$.
- 2) The delay of DATA is the same as the delay of SPACER, i.e., $D_{data} = D_{spacer} = D$. This assumption requires that the rising time of the circuit is equal to its falling time.
- 3) $D < T_{data+spacer}$ so that no two consecutive samples are missed. This assumption makes sure of a miss rate no more than 50%.

Without the loss of generality, request signals are initially set to high to request DATA. From Fig.5, it can be observed that the effect of the time difference Δt accumulates until a sample (DATA or SPACER) is missed, where

$$\Delta t = D - 0.5T_{data+spacer} \quad (2)$$

Furthermore, let n be defined by

$$n = \left\lfloor \frac{0.5T_{data+spacer}}{\Delta t} \right\rfloor \quad (3)$$

where $\lfloor x \rfloor$ is the floor function of x . Note that $n \geq 1$ due to assumption (3). It is also noted that a DATA sample is missed and two SPACERs are merged when n is odd, and a SPACER sample is missed and two DATA samples are merged when n is even.

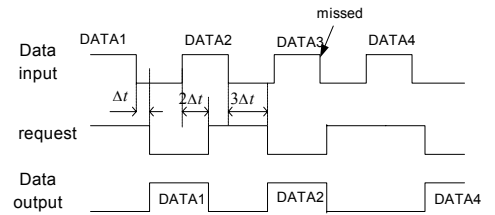


Fig. 5 Timing diagram under ULSV

When n is odd, a DATA missing is equivalent to a miss of a (DATA, SPACER) pair. When n is even, the two DATA samples separated by the missed spacer will merge, and thus the corresponding output is generally incorrect. Therefore, the information of two consecutive data samples is lost due to the spacer missing. However, we can modify the design of the first register to avoid DATA merging. Only the first DATA sample is allowed to pass through the modified register during the high voltage level of the input request signal so that the following DATA sample to be merged is blocked. For this purpose, only

register 1 needs to be modified by replacing 2-input C-elements in a traditional register by 3-input C-elements and connecting the third inputs of these 3-input C-elements to the acknowledge signal of its own, as shown in Fig.6. Thus, even when n is even, a SPACER missing can also be viewed as a miss of a (DATA, SPACER) pair using the modified register.

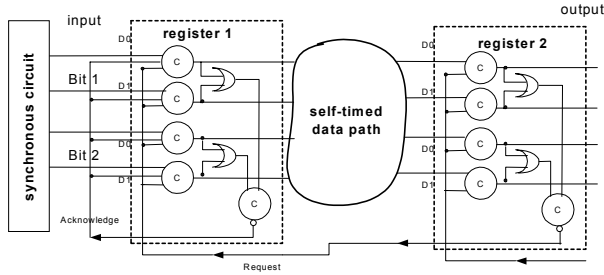


Fig. 6 the modified architecture without DATA merging

If there is a (DATA, SPACER) pair missed after every k pairs of (data, spacer) are delivered, then the miss rate of (DATA, SPACER) pair is defined by

$$R_m = \frac{1}{k+1} \quad (4)$$

where

$$k = \begin{cases} \frac{n+1}{2} & n \text{ is odd} \\ \frac{n}{2} + 1 & n \text{ is even} \end{cases} \quad (5)$$

where n is defined by (3). Obviously, the miss rate is a two-dimensional function of input data rate and circuit delay (or supply voltage). By defining the input data rate f as the reciprocal of the DATA-SPACER cycle $T_{data+spacers}$, replacing D in (2) by $D(V_{dd})$ [8], and combining (2), (3), (4), and (5), the miss rate in (4) can be rewritten as

$$R_m(V_{dd}, f) = \begin{cases} 1/2 & , 1 \leq \frac{1}{2f \cdot D(V_{dd}) - 1} < 2 \\ \frac{1}{k+1} & , 2(k-1) \leq \frac{1}{2f \cdot D(V_{dd}) - 1} < 2k, k = 2, 3, 4, \dots \\ 0 & , 2f \cdot D(V_{dd}) \leq 1 \end{cases} \quad (6)$$

where

$$D(V_{dd}) = \frac{C_L V_{dd}}{\beta(V_{dd} - V_t)^\alpha} \quad (7)$$

C_L is the total node capacitance,
 β is gate transconductance,
 V_t is the device threshold voltage.

Since a self-timed circuit has a characteristic of average-case delay, instead of worst-case delay, $D(V_{dd})$ in (6) is a average delay in real operation environments.

As an example, the miss rate $R_m(V_{dd}, f)$ for a chain of 8 full adders is plotted in Fig.7, where the plane (V_{dd}, f) is partitioned into different regions, and each region corresponds to a miss rate of (DATA, SPACER) pair. Given an input data rate, the supply voltage can be reduced significantly by allowing a tolerable miss rate. Similarly, given a supply voltage, the maximal input data rate can be increased by allowing a tolerable miss rate. The curve "critical V_{dd} " shows the minimal supply voltage for no-error operation.

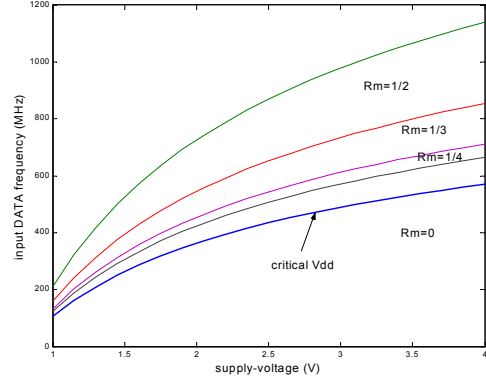


Fig. 7 Miss rate as a function of data rate and supply-voltage

4. APPLICATION FOR LOW POWER DSP

This ultra-low supply voltage scaling is particularly useful in systems with highly sequential algorithms that perform a large number of computation steps per data sample [9]. Consider a self-timed circuit, which performs speech signal processing, shown in Fig. 8. Since no consecutive DATA samples are missed, one bit flag DATA0 and DATA1 can be attached to two consecutive DATA samples respectively for miss detection. This flag bit passes from the input register to the output one without processing. If two consecutive outputs have the same flag DATA0 (or DATA1), there must be an output missed between these two consecutive outputs. The missed output is estimated by the interpolation based on the outputs delivered by the self-timed circuit. A simple interpolation method is adopted in this paper. The average of two consecutive outputs with the same flag is the estimation of the missed output.

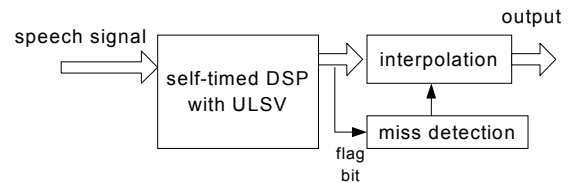


Fig. 8 Self-timed circuit for low power DSP application

A typical speech signal and its spectrum are plotted in Fig. 9. The magnitude of estimation error, normalized to input signal, is measured by

$$M_{error} = 20 \cdot \lg\left(\frac{\sigma_{error}}{\sigma_{signal}}\right) \quad (8)$$

where σ_{error}^2 is the variance of error and σ_{signal}^2 is the variance of input signal. Fig.10 shows the estimation error versus the reciprocal of miss rate for several types of speech signal. The error will decrease with the decrease of miss rate. The bandwidth of input signal also affects the error, thus increasing the SNR of input signal will reduce the estimation error.

As a case study, the delay of a self-timed circuit for the speech signal processing is modeled by (7) where $\alpha=1.1967$, and $C_L / \beta = 0.899 \cdot 10^{-9} F \cdot V^2 / A$, $V_t=0.75V$, based on $0.18\mu\text{m}$ CMOS technology. The reduction in power dissipation is characterized by power savings (PS) defined as

$$PS = \frac{P_{critical} - P_{ULSV}}{P_{critical}} \quad (9)$$

where $P_{critical}$ is the power dissipation with $V_{dd}=V_{critical}$, and P_{ULSV} is the power dissipation with V_{dd} less than $V_{critical}$. Neglecting the power dissipated by the error compensation circuit, the curves of power savings due to ULSV are plotted in Fig.11 for input DATA rate 200 MHz, 400 MHz, 600 MHz respectively. More than 40% to 70 % power can be saved by introducing -15dB to -10 dB error, which is tolerable in many DSP applications.

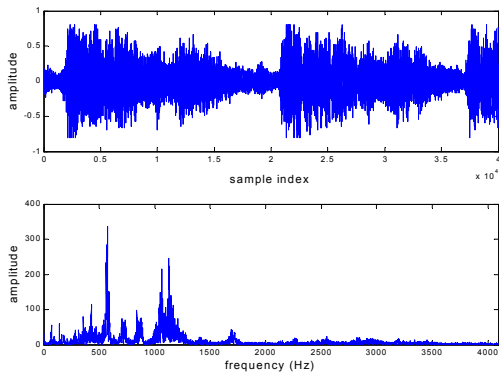


Fig. 9 A typical speech signal and its spectrum

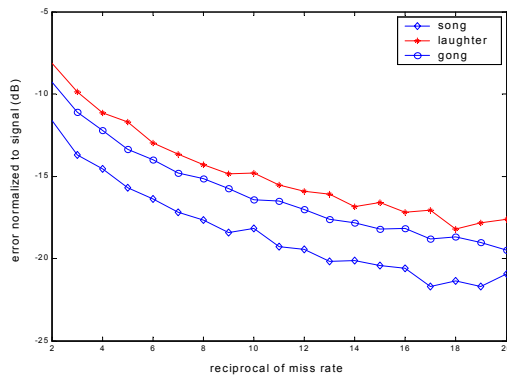


Fig.10 Error versus the reciprocal of miss rate

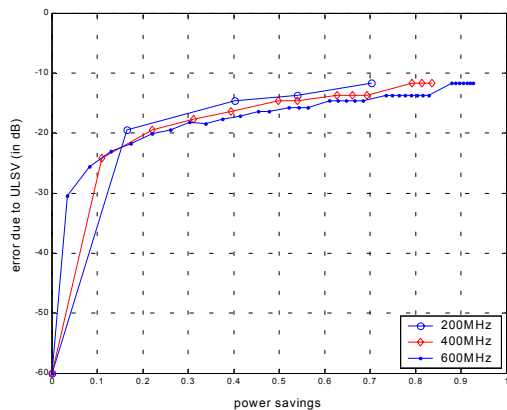


Fig.11 error versus power savings

5. CONCLUSION

In this paper, we have proposed an approach to low voltage low power design for DSP applications. This approach exploits the robustness of self-timed circuit to ULSV to achieve significant power saving. The effectiveness of this approach is demonstrated by miss rate analysis and a DSP case study. However, the bandwidth and SNR of input signal limit the

accuracy of error correction. On the other hand, the accuracy can be improved by a smaller miss rate and an advanced interpolation method such as linear prediction based on multi-samples. This improvement for accuracy will require an increasing of power dissipation.

6. REFERENCE

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