

Soft Digital Signal Processing Using Self-Timed Circuits

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Abstract In this paper, we propose a self-timed architecture for low power digital signal processing with ultra-low supply voltage. Compared to synchronous circuits, self-timed circuits are more robust at very low voltage. In many signal-noise-ratio (SNR)-required digital signal processing applications, this robustness allows the circuit to operate with very low supply voltage, even if some data samples are missed due to this low voltage. The missing leads to an SNR degradation. The degradation depends on input data frequency, supply voltage, specific circuit architecture, and process technology. Simulation shows that more than 40% to 70% power can be saved by introducing -15dB to -10 dB error in a case study: speech signal processing.

I. INTRODUCTION

SCALING of supply voltage leads to an aggressive power saving as well as an increased delay [1]. A lower bound of supply voltage $V_{critical}$ exists for the path delay corresponding to the throughput requirement. Erroneous operations probably happen when an ultra-low supply voltage (ULSV), a voltage less than $V_{critical}$, is applied. Fortunately, a moderate degradation due to the erroneous operations can be viewed as the introduction of noise, and thus is usually allowed in many digital signal processing (DSP) systems dealing with noise [2]. This fact leads to a tradeoff between the output signal-to-noise ratio (SNR) and power performance.

This tradeoff was implemented by synchronous DSP architectures in [3], referred to as *soft digital signal processing*. Consider an N-bit ripple carry adder as a block clocked by a synchronous clock with period T_s . If the delay of a single full-adder is T_{FA} , then the critical path delay of the N-bit adder is given by $T_{critical} = N \cdot T_{FA}$. If $T_{critical}$ is increased beyond T_s , due to the

reduction of supply voltage for power saving, the outputs for some inputs are incorrect while the outputs for other inputs are still correct. The erroneous outputs will be detected and partially compensated for via DSP techniques. However, the application of this technique is limited by the following factors: 1) the applied circuit must have a characteristic of delay data-dependency; 2) the probability of the erroneous outputs depends not only on the supply-voltage but also on the distribution of inputs, and a high probability of the erroneous outputs may degrade the accuracy of the final outputs to an unacceptable degree even after compensation.

Compared to synchronous circuits, totally different phenomena will happen when an ULSV is applied to a self-timed circuit. For the self-timed circuit with ULSV addressed in this paper, each output delivered is correct though some outputs are missed. It is easier to compensate for the missing output due to ULSV in self-timed circuits than for the erroneous outputs in the synchronous counterpart.

In this paper, the soft digital signal processing for low power is investigated in self-timed circuits. A self-timed architecture is proposed to achieve low power performance via soft DSP. The behavior of the architecture is analyzed and simulated when an ULSV is applied.

II. SELF-TIMED ARCHITECTURE

In this section, a self-timed architecture is proposed. In this architecture, dual-rail encode scheme is employed to achieve speed independency.

The self-timed circuit to be addressed is speed independent, where each bit of the data is encoded by dual rails (D0, D1), shown in Fig. 1. The state DATA 0 (D0=1, D1=0) corresponds to a Boolean logic 0. The DATA 1 (D0=0, D1=1) corresponds to a Boolean logic 1. SPACER

(D0=0, D1=0) corresponds to the empty set meaning that value of the bit is not yet available. The state (D0=1, D1=1) is forbidden. The data from synchronous system are synchronized at register 1 by request signal before entering the self-timed computation circuit. Another self-timed computation circuit can be connected to the output of register 2 to form a pipeline architecture, or a terminal, such as a monitor or D/A converter, can be used to receive the data out of register 2.

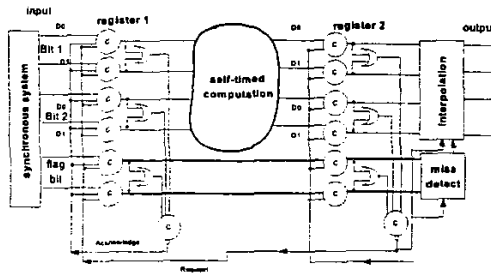


Fig. 1 The proposed architecture for soft DSP (Only two bits in data bus for simplicity)

In order to achieve speed independency, the data path must work under Seitz's weak condition [4]. Some techniques, such as differential cascode voltage switch logic (DCVSL) [5] and NULL convention logic (NCL) [6], can be employed to design the self-timed computation block. Martin's delay-insensitive full adder [7] can also be used in the data path. As shown in Fig.1, a register is composed of C-elements and OR gates. Considering register 1, if the request signal from register 2 is high to request DATA, then DATA is allowed to pass through register 1, and when each bit is DATA, the acknowledge signal will become low to request SPACER from the pre-stage, which means the computation is finished and the circuit needs to be reset. Similarly, if the request signal from register 2 is low to request SPACER, then SPACER is allowed to pass through register 1, and when all of bits are SPACERS, the acknowledge signal will become high to request another DATA from the pre-stage, which means the reset is finished and the circuit can start another computation.

In many applications, the input data of the self-timed come from a synchronous system,

such an A/D converter, and the data rate is constant and independent of the delay of the self-timed circuit. However, the allowed maximum input data rate is limited by the speed of the self-timed circuit. The timing constraint is illustrated in Fig. 2, where $T_{data+spacer}$ is the input DATA-SPACER cycle, D_{data} is the propagation delay of data from register 1 to register 2, which includes the delays of two registers and the data path, similarly D_{spacer} is the propagation delay of spacer from register 1 to register 2. The sum of D_{data} and D_{spacer} must be less than or equal to $T_{data+spacer}$, i.e.,

$$T_{data+spacer} \geq D_{data} + D_{spacer} \quad (1)$$

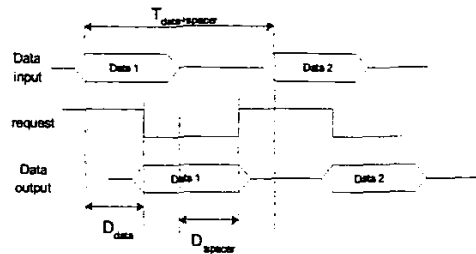


Fig.2 Timing constraint of self-timed circuit

III. MISS RATE IN SELF-TIMED CIRCUITS

The effect of ULSV on self-timed circuit is totally different from that on synchronous circuit described in [3]. When an ULSV is applied to a self-timed circuit, inequality (1) is violated. The following analysis shows that under the condition of ULSV the self-timed circuit would miss some input samples (DATA or SPACER), and the outputs corresponding to the inputs not missed are always correct. In other words, an output is either lost or delivered correctly.

For the sake of simplicity, we make the following assumptions:

- 1) The data rate of input is fixed, and the duration of DATA is equal to that of SPACER, i.e., $T_{data} = T_{spacer} = 0.5 T_{data+spacer}$.
- 2) The delay of DATA is the same as the delay of SPACER, i.e., $D_{data} = D_{spacer} = D$. This assumption requires that the rising time of the circuit is equal to its falling time.
- 3) $D < T_{data+spacer}$ so that no two consecutive samples are missed. This assumption makes sure of a miss rate no more than 50%.

It can be observed that the effect of the time difference Δt accumulates until a sample (DATA or SPACER) is missed, where

$$\Delta t = D - 0.5T_{data+spacer} \quad (2)$$

Furthermore, let n be defined by

$$n = \left\lfloor \frac{0.5T_{data+spacer}}{\Delta t} \right\rfloor \quad (3)$$

where $\lfloor x \rfloor$ is the floor function of x . Note that $n \geq 1$ due to assumption (3).

If there is a (DATA, SPACER) pair missed after average k pairs of (DATA, SPACER) are delivered at output, then the miss rate of (DATA, SPACER) pair is defined by

$$R_m = \frac{1}{k+1} \quad (4)$$

where k is given by

$$k = \frac{n+1}{2} \quad (5)$$

where n is defined by (3). Note that k is not necessarily an integer. Obviously, the miss rate is a two-dimensional function of input data rate and circuit delay (or supply voltage). By defining the input data rate f as the reciprocal of the DATA-SPACER cycle $T_{data+spacer}$, replacing D in (2) by $D(V_{dd})$, and combining (2), (3), (4), and (5), the miss rate in (4) can be rewritten as

$$R_m(V_{dd}, f) = \frac{2}{n+3}, \quad n \leq \frac{1}{2f \cdot D(V_{dd}) - 1} < n+1, \quad n=1,2,3,\dots \quad (6)$$

where

$$D(V_{dd}) = \frac{C_L V_{dd}}{\beta(V_{dd} - V_t)^a} \quad (7)$$

C_L is the total node capacitance,

β is gate transconductance,

V_t is the device threshold voltage.

The circuit delay is estimated by (7) with a good accuracy [8]. Since a self-timed circuit has a characteristic of average-case delay, instead of worst-case delay, $D(V_{dd})$ in (6) is a average delay in real operation environments.

As an example, the miss rate $R_m(V_{dd}, f)$ for a chain of 8 full adders is plotted in Fig.3, where the plane (V_{dd}, f) is partitioned into different regions, and each region corresponds to a miss rate of (DATA,SPACER) pair. Given an input data rate, the supply voltage can be reduced significantly by allowing a tolerable miss rate. Similarly, given a supply voltage, the maximal input data rate can be increased by allowing a tolerable miss rate. The curve "critical V_{dd} "

shows the minimal supply voltage for no-error operation.

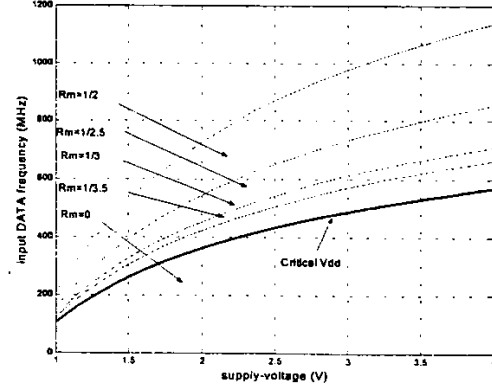


Fig.3 Miss rate as a function of data rate and supply-voltage

IV. SIMULATION RESULTS

This ultra-low supply voltage scaling is particularly useful in systems with highly sequential algorithms that perform a large number of computation steps per data sample [9]. Consider a self-timed circuit, which performs speech signal processing, shown in Fig. 1. Since no consecutive DATA samples are missed under assumption (3), one bit flag DATA0 and DATA1 can be attached to two consecutive DATA samples respectively for miss detection. This flag bit passes from the input register to the output one without processing. If two consecutive outputs have the same flag DATA0 (or DATA1), there must be an output missed between these two consecutive outputs. The missed output is estimated by the interpolation based on the outputs delivered by the self-timed circuit. A linear interpolation method is adopted in this paper. The average of two consecutive outputs with the same flag is the estimation of the missed output.

A typical speech signal $y(n)$ and its spectrum without missing are plotted in Fig. 4. The output $\hat{y}(n)$ from the interpolation includes the ideal output signal $y(n)$ and error signal $e(n)$, expressed by

$$\hat{y}(n) = y(n) + e(n) \quad (8)$$

The magnitude of interpolation error, normalized to ideal output signal, is defined by

$$M_{error} = 20 \cdot \lg\left(\frac{\sigma_{error}}{\sigma_y}\right) \quad (9)$$

where σ_{error}^2 is the variance of error $e(n)$ and σ_y^2 is the variance of ideal output signal $y(n)$. Fig.5 shows the estimation error versus the reciprocal of miss rate for several types of speech signal. The error depends on the bandwidth of signal, interpolation method, and miss rate.

where $P_{critical}$ is the power dissipation with $V_{dd}=V_{critical}$, and P_{ULSV} is the power dissipation with V_{dd} less than $V_{critical}$. Neglecting the power dissipated by the error compensation circuit, the curves of power savings due to ULSV are plotted in Fig.7 for input DATA rate 200 MHz, 400 MHz, 600 MHz respectively. More than 40% to 70 % power can be saved by introducing -15dB to -10 dB error, which is tolerable in many DSP applications.

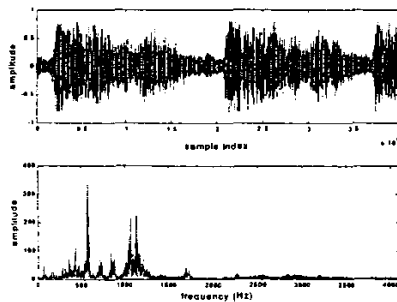


Fig. 4 A typical speech signal and its spectrum

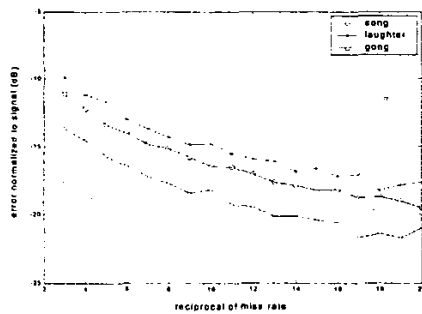


Fig.5 Error versus the reciprocal of miss rate

As a case study, the delay of a self-timed circuit for the speech signal processing is modeled by (7) where $\alpha=1.1967$, and $C_L/\beta = 0.899 \cdot 10^{-9} F \cdot V^2/A$, $V_t=0.75V$, based on $0.18\mu\text{m}$ CMOS technology. Given an input DATA frequency, the error magnitude M_{error} is plotted in Fig.6 as a function of supply voltage. The reduction in power dissipation is characterized by power savings (PS) defined as

$$PS = \frac{P_{critical} - P_{ULSV}}{P_{critical}} \quad (10)$$

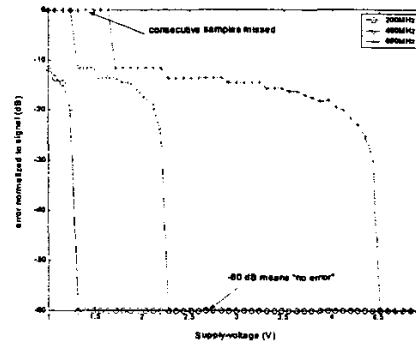


Fig.6 Error versus supply voltage

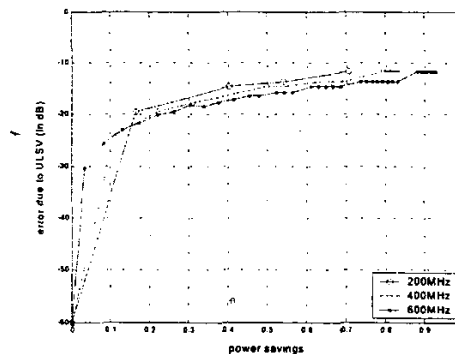


Fig.7 Error versus power savings

V. CONCLUSION

In this paper, we have proposed an approach to low voltage low power design for DSP applications. This approach exploits the robustness of self-timed circuit to ULSV to achieve significant power saving. The effectiveness of this approach is demonstrated by miss rate analysis and a DSP case study. However, the bandwidth and SNR of input signal

limit the accuracy of error correction. On the other hand, the accuracy can be improved by a smaller miss rate and an advanced interpolation method such as linear prediction based on multi-samples and data autocorrelation [2]. This improvement for accuracy will require an increasing of power dissipation.

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