

A Low Power Domino with Differential-Controlled-Keeper

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Abstract— Domino circuits are used to achieve higher system performance than static CMOS techniques. This work briefly surveys domino keeper designs for high fan-in domino circuits. A new domino circuit structure is shown in this paper that reduces the Power-Delay-Product over 16% as compared to previous domino techniques with keepers.

I. INTRODUCTION

Domino circuits can be used in the critical path to increase the speed of the circuit. Different domino techniques have been developed to increase performance [1-6]. The keeper is required in domino circuits to keep the state from being destroyed by leakage. The downside, however, of the keeper is that it will fight the pull down network at the beginning of the evaluation.

There are several categories of keeper designs for footless domino:

1. simple keeper(without clock delay structure)
2. clock delayed single keeper
3. clock delayed dual keepers.

In the simple keeper structure, the keeper will content with the signal at the beginning of the evaluation which degrades the speed. The clock delayed single keeper does not content at the beginning of the evaluation. In the clock delayed dual keepers there are two keepers, one strong, one weak, this dual keeper structure essentially combines the previous two structures. This work will show an improved dual keepers structure for low power consumption.

This paper is organized as follows. Section I presented the introduction. Sections II surveys the previous designs and categories them into three types. Section III describes the proposed differential keeper technique. Section IV shows the simulation results comparing the proposed design with other designs shown here. Section V presents a summary of the paper.

II. PREVIOUS DESIGNS

A. Simple Keeper Domino

Traditional domino circuits have a clocked NMOS transistor, which is necessary if any of the inputs are not produced by a preceding domino circuit. A class of domino circuits called “footless” domino, as shown in Fig. 1, removes the clocked evaluation NMOS transistor from the traditional domino to improve the speed of the circuit. This may cause an extended precharge cycle because the precharge state must then propagate through each domino stage [1]. However, the clock can be delayed between stages to ensure that each stage has a precharged (low) output before the subsequent stage starts precharge. This prevents the pull-up and pull-down network from contention.

A domino circuit having only one PMOS transistor as the keeper characterizes the simple keeper category. This category covers both a single PMOS keeper driven either from X through a separate inverter as in Fig. 2, or driven directly by output Q. Simple keepers are further discussed in [1].

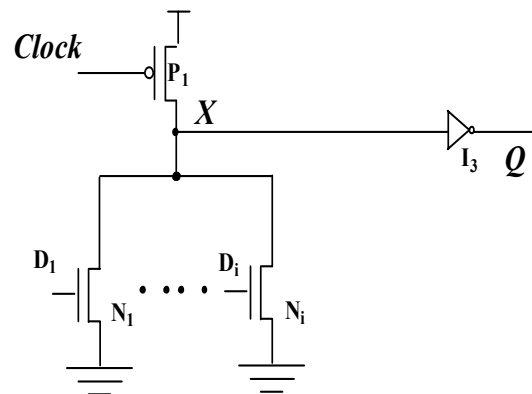


Fig.1 Footless Domino

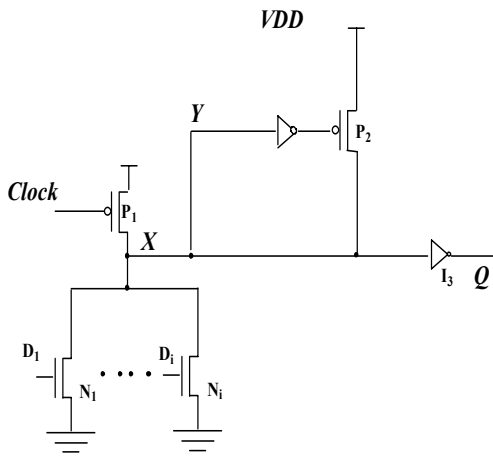


Fig. 2. Simple Keeper Domino

During evaluation, the clock will be high. If the inputs $D_1 \dots D_i$ are Low, node X should remain at its precharged state of High. However, due to leakage currents when there are many NMOS evaluation transistors in parallel (i is large for D_i), leakage currents will flow to ground causing X to slowly discharge. The simple keeper P2 will keep X high during evaluation if all inputs are 0.

The simple keeper will always be active at the beginning of evaluation because X is initially high. If any input is high, and X tries to go low, P2 will fight against it for a short time. Hence, a basic tradeoff exists here, which is the sizing of P2. A small sized P2 may not fight the leakage, but a large sized P2 may hinder the speed during evaluation.

B. Clock Delayed Single Keeper

Another solution is the clock delayed single keeper style, which is shown in Fig. 3 [2]. A domino circuit having a single keeper being driven by a combination of the output node and a delayed clock characterizes this category. The particular design shown in Fig. 3 is called High Speed Domino [2]. The keeper in this category is not active at the start of the evaluation stage. Therefore, the keeper size can be made large to accommodate the leakage, without the keeper transistor fighting with the internal node X at the beginning of the evaluation cycle. Basically, the keeper is active only after 2 inverter delays when evaluation begins if the output is low.

At the evaluation phase, CLK_N+1 will stay low for 2 inverter delays causing M3 to stay on, which pulls A to high. This turns keeper P1 off. After the 2 inverter delays of time have passed, CLK_N+1 is high which turns on M2. If the evaluation node is high, then A is zero, P1 will turn on to keep the evaluation node high, fighting the effects of leakage. Note, however, that during the 2 inverter delay at the beginning of evaluation, the keeper is inactive, making the evaluation node floating, subjecting the node to noise and affecting the design robustness [5,4]. Further, when clk_N+1

is Vdd and out node is Vdd, A goes to $V_{dd}-V_{th}$ and not Vdd causing higher leakage current though the keeper transistor.

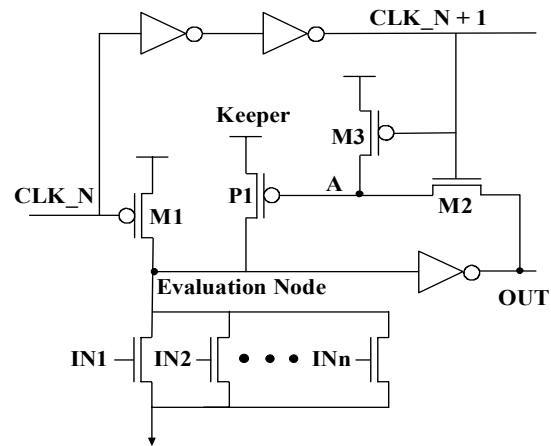


Fig. 3. High Speed Domino

C. Clock Delayed Dual Keepers

The third category is the clock delayed dual keepers designs. The delayed clock is used in control of the keepers. Domino circuits in this category contain two different keepers. One keeper is weak, and the other is strong. This type of design is used to reduce the overhead on speed while strongly resisting the leakage current after evaluation.

1) NAND Keeper Domino

The NAND keeper domino is of this type, as shown in Fig. 4 [3]. The NAND Keeper uses a strong and weak keeper to balance leakage current, overhead, and speed. The strong keeper P2 is only activated when needed during the evaluation mode (Clock is high and X is high) after some delay. This prevents noise from destroying the value of X. Also, the weak keeper P3 will be on anytime node X is high (i.e. before strong keeper P2 is active) to prevent noise problems between the time evaluation begins and the time strong keeper P2 is activated. Initially during an evaluation,

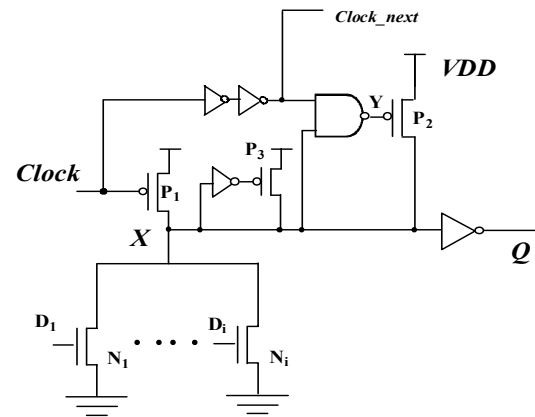


Fig. 4. NAND Keeper Domino

the small keeper P3 prevents node X from floating. It is weak and will not affect evaluation very much. After some time, strong keeper P2 will be activated and ensure that node X does not fail due to leakage.

2) Series PMOS Domino

Another type of clock delayed dual keeper is the series PMOS domino shown in Fig. 5 [4].

The Series PMOS Domino circuit is similar to the NAND keeper in that it has two keeper transistors. However, it contrasts in the way the strong keeper (P2) operates. Also, the output rather than the evaluation node drives the weak keeper as it is in the NAND keeper design. The weak keeper P1 is on when evaluation begins, but P2 is off. Node A starts at high and stays that way until a delay of 2 inverters plus inverter delay logic has lapsed. Afterwards, A will allow keeper P2 to operate. So if the output node is low, keeper P2 will be on as long as A is low.

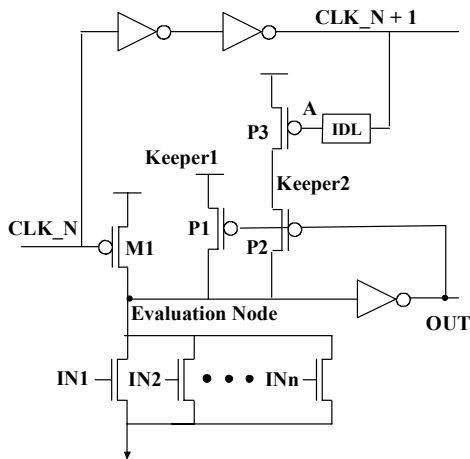


Fig.5 Series PMOS Domino

III. PROPOSED DESIGN

Simple keeper structure has contention problem at the beginning of the evaluation. The clocked delayed keeper has floating node at the beginning of the evaluation. The dual keeper structure combines the previous two techniques by using two keepers, hence the power consumption will increase. This work shows an improved clock delayed dual keeper structure for low power consumption which we call differential controlled keeper domino circuit, Fig. 6. The weak keeper is P5 and the strong keeper is P2. Keeper P2 constructs a differential structure with P4.

Assume all inputs D1 to Di are low. During precharge, the clock goes low. When this occurs, node X is driven high and node Y is driven high. Then Q goes low. Because Q is low and Y is high, node Z is driven to high, which ensures that the strong keeper P2 is off. Thus, the strong keeper is

disconnected during the precharge cycle. However, since Q is low, the weak keeper P5 is on. So the strong keeper is always off during precharge, while the weak keeper is on during precharge.

If the inputs all stay low during evaluation, the strong keeper will turn on. First the clock will transition to high indicating evaluation. This causes node Y to go low which makes node Z go low. This activates the strong keeper P2 to help keep node X high, giving assistance to the small keeper P5. Therefore both keepers are active during evaluation when all inputs remain low.

During evaluation if any set of inputs goes high and causes node X to go low, the following occurs. First, node X is driven low. X being low causes P4 to turn on while P3 is turned off because Q is high. Therefore, the strong keeper P2 is disconnected and weak keeper P5 is disconnected. Both keepers disconnect when the pulldown network is active.

The PMOS transistor P3 is basically a switch that decides when strong keeper P2 should be enabled. It is controlled by the output Q and is always turned on when node X is high. So whenever node X is high, the decision to turn on the strong keeper is based on the inverted value of the clock. When switch P3 is off (node X is low), transistor P4 forces the strong keeper to stay off.

When the clock goes to Vdd, the inputs are still at 0V because it is a footless domino circuit. After a certain delay dependent on the design of the driving domino circuits and the clock delay, the inputs may go high. If this delay is larger than the delay of the inverter driving node Y, then Y will go to 0V while Q is still at 0V thereby turning P2 on before evaluation completes

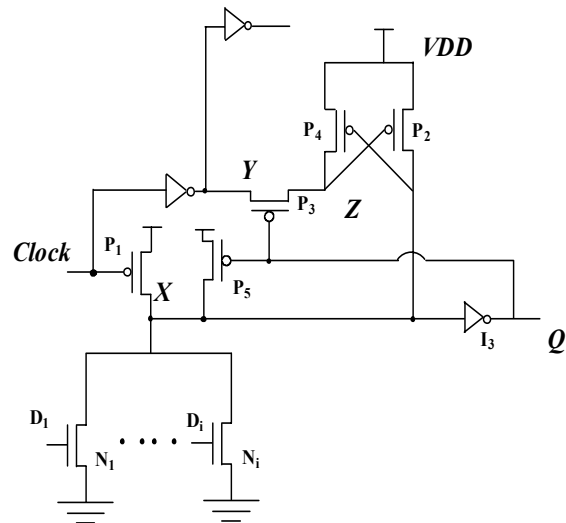


Fig. 6 Proposed Differential Controlled Keeper Domino

IV. SIMULATION RESULTS

Simulation results were obtained in HSPICE using 0.18 μ m CMOS technology at room temperature. Parasitic capacitances were extracted from layouts. The large capacitance of the internal node due to the high fan-in NMOS network is included by using the layouts of each design for simulation. The circuits were simulated in a cascading domino environment in order to achieve accurate results, as shown in Fig. 7.

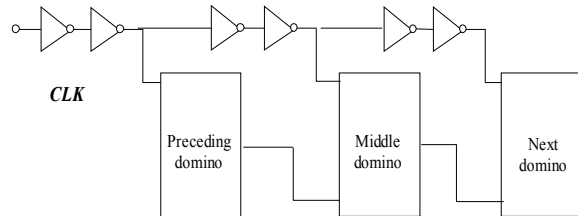


Fig. 7 Simulation Environment

The preceding domino block drives the middle domino block and the output of the middle domino is driving the last domino. Delay is measured from the middle domino block. Power consumption is measured when one input goes high and discharges the precharge node in every evaluation phase similar to the method in [5].

The transistors for the two keepers are sized according to the ratio of the current driving capability of the keeper versus the driving ability of one of the pull down evaluation transistors. The keeper ratio, K , is defined as

$$K = (W/L)_{\text{keeper}} / (W/L)_{\text{evaluation}}$$

The small keeper has the ratio K of 0.1, while the large keeper has a ratio of 0.4, similar to that of [5].

The designs were compared using the parameters of number of transistors (excluding pull down network), number of clocked transistors, delay, power, and power-delay-product. The results of the simulations are shown in Table I.

The proposed differential domino circuit shows a reduction in power consumption as compared to the other designs. The savings in power is a result of the efficient keeper topology. In the series PMOS design, two PMOS transistors are in series. In order to have an adequate driving capability for the keeper, the sizes of these two PMOS should be doubled. This increases the power and delay overhead. The NAND Keeper design has 4 transistors that control the strong keeper. However, in the proposed differential domino, only 2 transistors (P3, P4) are needed to control the keeper. The reason the differential domino has the lowest power is that it uses the least number of clocked transistors as well as the least number of overall transistors. It reduces PDP by 16% over the NAND keeper domino.

The NAND keeper has the smallest delay of all the designs because it has no additional output load, whereas in

TABLE I. RESULTS

Design Name	# of Transistors	# of clocked Transistors	Delay (ps)	Power (uW)	PDP (fJ)
NAND Keeper	15	7	231	290	67.0
Series PMOS	12	8	293	288	84.4
Proposed Differential	11	6	246	234	57.6

the other designs the keepers are controlled by the output. The proposed design has the second best delay. The series PMOS design, having the two PMOS in series for the strong keeper, increases its delay. Considering the PDP, the proposed differential keeper has the best (smallest) among all the designs.

V. SUMMARY

The proposed differential keeper domino design has been compared with some previously published domino circuits. All designs have been categorized into three groups: the simple keeper, clock delayed keeper, and dual keepers.

This new design uses an efficient topology to achieve the delayed keeper structure. In addition, the design has less clocked transistors and less overall transistors than the other designs. The power and power delay product is better than the other designs as well. This makes the design suitable for low power and high performance applications.

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